AMENDMENT

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer, and Assignee reserves the right to claim this subject matter in a continuing application:

1. (Currently Amended) ~~A circuit~~ An apparatus ~~with General Purpose Input Output (GPIO) pins~~, comprising:

a scanner memory~~, which has a~~ having a plurality of memory ~~pin~~ pins ~~and is refreshed by a recharging signal to maintain stored data in the memory~~;

a control processing unit having a plurality of data ~~pin~~ pins, wherein at least one of the plurality of data ~~pin~~ pins is coupled to at least one of the plurality of memory ~~pin~~ pins; and

a buffer, coupled to at least one of the plurality of data ~~pin~~ pins, wherein the buffer is adapted to ~~for receiving an input signal and feeding the input signal into~~ provide data signals to the at least one of the plurality of data pins ~~the control processing unit~~ according to a control signal synchronized with ~~the~~ a recharging signal provided to the scanner memory.

2. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 1, wherein the control processing unit ~~is~~ comprises an Application Specific Integrated Circuit (ASIC).

3. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 1, wherein the ~~buffer's~~ buffer comprises a model ~~is~~ 74HC/HCT244 buffer.

4. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 1, wherein the scanner memory ~~is~~ comprises ~~a~~ Dynamic Random Access Memory.

5. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 1, wherein the control signal is ~~sent from~~ provided by the control processing unit.

6. (Currently Amended) ~~A circuit~~ An apparatus ~~with General Purpose Input Output (GPIO) pins~~, comprising:

a scanner memory~~, which has a~~ having a plurality of memory ~~pin~~ pins ~~and is refreshed by a recharging signal to maintain stored data in the memory~~;

a control processing unit having a plurality of data ~~pin~~ pins, wherein at least one of the plurality of data ~~pin~~ pins is coupled to at least one of the plurality of memory ~~pin~~ pins; and

a buffer, coupled to one or more of the plurality of data ~~pin~~ pins, wherein the buffer is adapted to receive ~~for outputting~~ an output signal provided from one or more of the plurality of data pins ~~the control processing unit~~, wherein the buffer outputs the output signal according to a control signal synchronized with ~~the~~ a recharging signal provided to the scanner memory.

7. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 6, wherein the control processing unit ~~is~~ comprises an Application Specific Integrated Circuit (ASIC).

8. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 6, wherein the ~~buffer's~~ buffer comprises a model ~~is~~ TC74HC374 buffer.

9. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 6, wherein the scanner memory ~~is~~ comprises ~~a~~ Dynamic Random Access Memory.

10. (Currently Amended) The ~~circuit~~ apparatus ~~with General Purpose Input Output (GPIO) pins~~ according to claim 6, wherein the control signal is ~~sent from~~ provided by the processing unit.

11. (New) The apparatus of claim 1, wherein the buffer is further adapted to receive data signals from one or more of the plurality of data pins according to a control signal synchronized with a recharging signal provided to the memory.

12. (New) The apparatus of claim 1, wherein at least a portion of the plurality of data pins comprise General Purpose Input Output (GPIO) pins.

13. (New) The apparatus of claim 1, wherein at least a portion of said data signals are provided to at least a portion of the plurality of data pins of the control processing unit substantially coincident with the recharging signal provided to the scanner memory.

14. (New) The apparatus of claim 6, wherein the buffer is further adapted to receive data signals from one or more of the plurality of data pins according to a control signal synchronized with a recharging signal provided to the memory.

15. (New) The apparatus of claim 6, wherein at least a portion of the plurality of data pins comprise General Purpose Input Output (GPIO) pins.

16. (New) The apparatus of claim 6, wherein at least a portion of said data signals are provided to at least a portion of the plurality of data pins of the control processing unit substantially coincident with the recharging signal provided to the scanner memory.

17. (New) A scanner, comprising:

a bus;

a buffer communicatively coupled to the bus,

a memory communicatively coupled to the bus, wherein the memory is adapted to receive a recharge signal; and

a control processing unit communicatively coupled to the bus, wherein the control processing unit is adapted to generate a control signal responsive to the recharge signal provided to the memory, to enable data transfer between the buffer and the control processing unit, wherein the data transfer is synchronized with the recharge signal provided to the memory.

18. (New) The scanner of claim 17, wherein the control processing unit comprises an Application Specific Integrated Circuit (ASIC).

19. (New) The scanner of claim 17, wherein the scanner memory comprises Dynamic Random Access Memory.

20. (New) The scanner of claim 17, wherein the buffer is further adapted to receive data signals from the control processing unit according to a control signal synchronized with a recharging signal provided to the memory.

21. (New) The scanner of claim 20, wherein the control processing unit further comprises a plurality of data pins adapted to provide the data signals to the buffer, wherein at least a portion of the data pins comprise General Purpose Input Output (GPIO) pins.

22. (New) A method of accessing a control processing unit of a scanning device, comprising:

providing an input signal to a buffer of the scanning device;

determining whether a recharge signal is being provided to a memory of the scanning device; and

enabling data transfer of at least a portion of the input signal between the buffer and the control processing unit, wherein the data transfer is synchronized with the recharge signal provided to the memory.

23. (New) The method of claim 22, wherein the control processing unit comprises an Application Specific Integrated Circuit (ASIC).

24. (New) The method of claim 22, wherein the scanner memory comprises Dynamic Random Access Memory.

25. (New) The method of claim 22, wherein the buffer is further adapted to receive data signals from one or more data pins of the control processing unit according to a control signal synchronized with a recharging signal provided to the memory.

26. (New) The method of claim 25, wherein at least a portion of the data pins comprise General Purpose Input Output (GPIO) pins.